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## (54) Data processing circuit, microcomputer, and electronic equipment

(57) The data processing circuit of this invention enables efficient description and execution of processes that act upon the stack pointer, using short instructions. It also enables efficient description of processes that save and restore the contents of registers, increasing the speed of processing of interrupts and subroutine calls and returns. A CPU that uses this data processing circuit comprises a dedicated stack painter register SP and uses an instruction decoder to decode a group of dedicated stack pointer instructions that specify the SP as an implicit operand. This group of dedicated stack pointer instructions are implemented in hardware by using general-purpose registers, the PC, the SP, an address adder, an ALU, a PC incrementer, internal buses, internal signal lines, and external buses. This group of dedicated stack pointer instructions comprises SP-relative load instructions, stack pointer move instructions, a call instruction, a ret instruction, a sequential push instruction, and a sequential pop instruction.

FIG. 1A

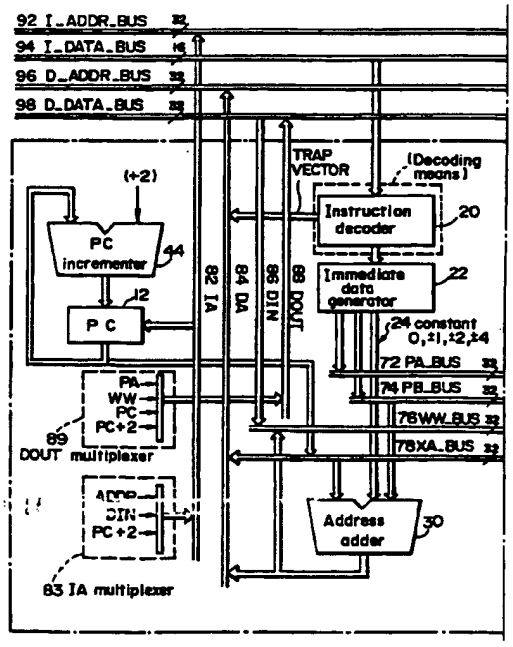


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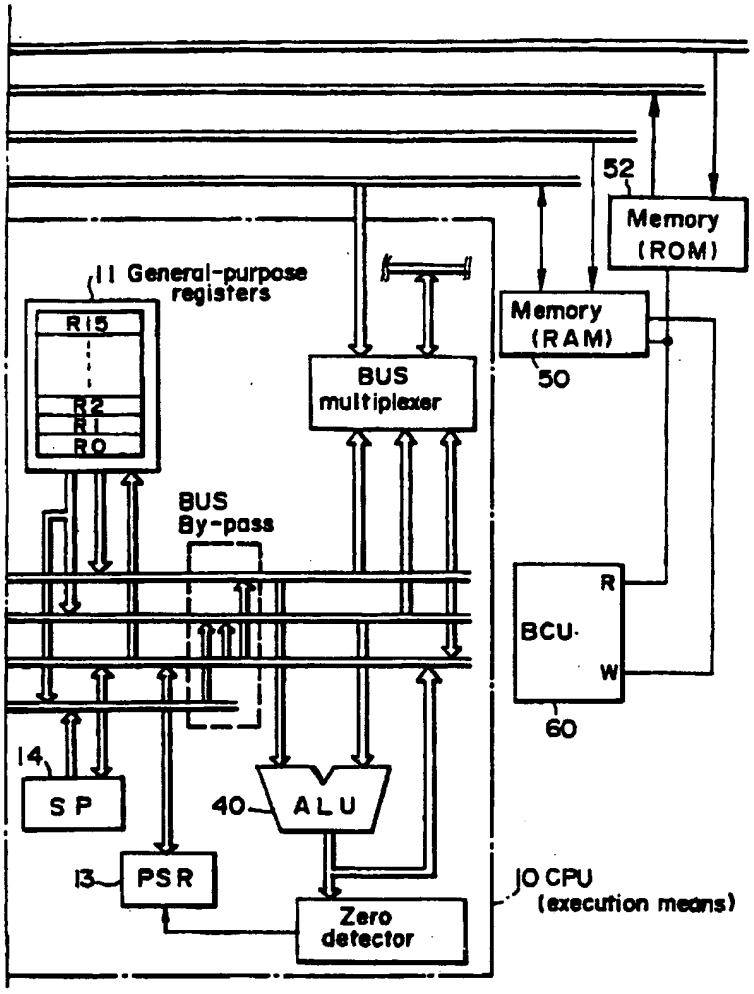
FIG. 1B


52
Memory (ROM)
11 General-purpose registers
R15
R2
R1
R0
Memory (RAM)
50
BUS multiplexer
BUS By-pass
R
BCU
W
60
14
SP
40
ALU
13
PSR
Zero detector
10 CPU (execution means)

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# EUROPEAN SEARCH REPORT

Application Number
EP 97 10 8346

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| X<br>Y<br>A | US 5 421 029 A (YOSHIDA TOYOHIKO) 30 May 1995<br>* column 11, line 29 - column 12, line 33 *<br>* column 25, line 40 - column 31, line 35 * | 1-4,11, 12,15-17<br>5,7<br>9,10 | G06F9/30<br>G06F9/40<br>G06F9/312 |
| Y<br>A | J. F. WAKERLY: "Micro-computer Architecture and Programming" 1981 , JOHN WILEY & SONS, INC. , NEW YORK, US XP002084210<br>* page 433 - page 437 *<br>* page 450 - page 453 * | 5<br>6 | |
| Y | WO 96 08767 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 21 March 1996<br>* page 2, line 31 - page 3, column 14 *<br>* page 4, line 10 - page 5, line 13 *<br>* page 8, line 17 - page 9, line 15 *<br>* page 11, line 15 - page 12, line 2 * | 7 | |
| X | US 4 236 206 A (HASTINGS THOMAS N ET AL) 25 November 1980<br>* column 14, line 56 - column 18, line 44 * | 1,11 | TECHNICAL FIELDS SEARCHED (Int.Cl.6)<br>G06F |
| A | FR 2 637 708 A (NIPPON ELECTRIC CO) 13 April 1990<br>* the whole document * | 8,9 | |
| A | STALLINGS W: "REDUCED INSTRUCTION SET COMPUTER ARCHITECTURE" PROCEEDINGS OF THE IEEE, vol. 76, no. 1, January 1988, pages 38-55, XP000027671<br>* page 42, left-hand column * | 13,14 | |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 12 November 1998 | Daskalakis, T |

CATEGORY OF CITED DOCUMENTS

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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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